We Claim:

1. A method of making an optoelectronic integrated circuit comprising:

forming isolation trenches in a SOI structure to form at least first and second isolated areas of silicon;

forming a first silicon island over the first silicon area during a first silicon forming step, wherein the first silicon island forms at least a portion of an optical device;

forming a second silicon island over the second silicon area during a second silicon forming step; and,

processing at least the second silicon area to form an electronic device with the second silicon island.

2. The method of claim 1 wherein the first silicon island comprises a poly-silicon island.

3. The method of claim 1 wherein the second silicon island comprises a poly-silicon island.

4. The method of claim 1 wherein the first silicon island comprises a first poly-silicon island, and

wherein the second silicon island comprises a second poly-silicon island.

5. The method of claim 1 wherein the first silicon island comprises an amorphous silicon island.

6. The method of claim 1 wherein the second silicon island comprises an amorphous silicon island.

7. The method of claim 1 wherein the first silicon island comprises a first amorphous silicon island, and wherein the second silicon island comprises a second amorphous silicon island.

8. The method of claims 1 wherein the forming of isolation trenches comprises forming LOCOS based dielectric isolation trenches.

9. The method of claims 8 further comprising vertically etching the SOI structure so as to form a vertical wall of a further optical device.

10. The method of claims 9 wherein the LOCOS based dielectric isolation trenches have sloped side walls.

11. The method of claims 1 wherein the forming of isolation trenches comprises forming shallow trench dielectric isolation trenches having vertical side walls.

12. The method of claims 11 further comprising vertically etching the SOI structure so as to form a vertical wall of a further optical device.

13. The method of claims 1 further comprising vertically etching the SOI structure so as to form a vertical wall of a further optical device.

14. The method of claim 1 wherein the forming of isolation trenches in a SOI structure comprises forming of an isolation trench at least partially filled with a dielectric, and wherein the forming of a first silicon island over the first silicon area comprises forming the first silicon island over the first silicon area and the dielectric.

15. The method of claim 1 wherein the forming of isolation trenches in a SOI structure comprises forming of an isolation trench so as to substantially expose a buried insulation layer of the SOI structure, and wherein the forming of a first silicon island over the first silicon area during a first silicon forming step comprises forming the first silicon island in over the first silicon area and the exposed buried insulation layer.

16. A method of making an optoelectronic integrated circuit comprising:

forming isolation trenches in a SOI structure to form at least first and second isolated areas of silicon;

forming a first silicon island over the first silicon area during a first silicon forming step, wherein the first silicon island forms at least a portion of an optical device;

forming a second silicon island over the second silicon area during a second silicon forming step, wherein the first and second silicon forming steps are separate silicon forming steps;

processing at least the second silicon area to form an electronic device with the second silicon island;

forming a blocking oxide over a first portion of the first silicon island so as to leave a second portion of the first silicon island exposed; and,

siliciding the second portion of the first silicon island, at least a portion of the second silicon area, and at least of portion of the second silicon island to form contact areas for the optical device and the electronic device.

17. The method of claim 16 wherein the first silicon island comprises a poly-silicon island.

18. The method of claim 16 wherein the second silicon island comprises a poly-silicon island.

19. The method of claim 16 wherein the first silicon island comprises a first poly-silicon island, and wherein the second silicon island comprises a second poly-silicon island.

20. The method of claim 16 wherein the first silicon island comprises an amorphous silicon island.

21. The method of claim 16 wherein the second silicon island comprises an amorphous silicon island.

22. The method of claim 16 wherein the first silicon island comprises a first amorphous silicon island, and wherein the second silicon island comprises a second amorphous silicon island.

23. The method of claims 16 wherein the forming of isolation trenches comprises forming LOCOS based dielectric isolation trenches.

24. The method of claims 23 further comprising vertically etching the SOI structure so as to form a vertical wall of a further optical device.

25. The method of claims 24 wherein the LOCOS based dielectric isolation trenches have sloped side walls.

26. The method of claims 16 wherein the forming of isolation trenches comprises forming shallow

trench dielectric isolation trenches having vertical side walls.

27. The method of claims 26 further comprising vertically etching the SOI structure so as to form a vertical wall of a further optical device.

28. The method of claims 16 further comprising vertically etching the SOI structure so as to form a vertical wall of a further optical device.

29. The method of claim 16 wherein the forming of a blocking oxide comprises forming spacers along the second silicon island.

30. The method of claim 16 wherein the forming of isolation trenches in a SOI structure comprises forming of an isolation trench at least partially filled with a dielectric, and wherein the forming of a first silicon island over the first silicon area comprises forming the first silicon island over the first silicon area and the dielectric.

31. The method of claim 16 wherein the forming of isolation trenches in a SOI structure comprises forming of an isolation trench so as to substantially expose a buried insulation layer of the SOI structure, and wherein the forming of a first silicon island over the first silicon area during a first silicon forming step comprises forming the first silicon island in over the first silicon area and the exposed buried insulation layer.

32. An optoelectronic device comprising:

a SOI structure having at least first and second trenches isolating at least first and second silicon areas;

an optical device formed over at least a portion of the first silicon area and a portion of the first trench, the optical device including a first silicon island;

an electronic device formed in and over the second silicon area, the electronic device including a second silicon island forming a gate region of the electronic device;

a first silicide region formed in the first silicon area and a second silicide region formed in the

first silicon island, wherein the first and second silicide regions form contacts for the optical device; and,

third and fourth silicide regions formed in the second silicon area and a fifth silicide region formed in the second silicon island, wherein the third, fourth, and fifth silicide regions form contacts for the electronic device.

33. The optoelectronic device of claim 32 wherein the first silicon island comprises a poly-silicon island.

34. The optoelectronic device of claim 32 wherein the second silicon island comprises a poly-silicon island.

35. The optoelectronic device of claim 32 wherein the first silicon island comprises a first poly-silicon island, and wherein the second silicon island comprises a second poly-silicon island.

36. The optoelectronic device of claim 32 wherein the first silicon island comprises an amorphous silicon island.

37. The optoelectronic device of claim 32 wherein the second silicon island comprises an amorphous silicon island.

38. The optoelectronic device of claim 32 wherein the first silicon island comprises a first amorphous silicon island, and wherein the second silicon island comprises a second amorphous silicon island.

39. The optoelectronic device of claims 32 wherein the first and second trenches comprise corresponding LOCOS based first and second dielectric trenches.

40. The optoelectronic device of claims 39 further comprising a third trench, wherein the third trench forms a vertical wall of a third silicon island of the SOI structure, and wherein the vertical wall comprises a further optical device.

41. The optoelectronic device of claims 40 wherein the LOCOS based first and second dielectric trenches have sloped side walls.

42. The optoelectronic device of claims 32 wherein the first and second trenches are formed as corresponding first and second shallow dielectric trenches having vertical side walls.

43. The optoelectronic device of claims 42 further comprising a third trench, wherein the third trench forms a vertical wall of a third silicon island of the SOI structure, and wherein the vertical wall comprises a further optical device.

44. The optoelectronic device of claims 32 further comprising a third trench, wherein the third trench forms a vertical wall of a third silicon island of the SOI structure, and wherein the vertical wall comprises a further optical device.

45. The optoelectronic device of claim 32 further comprising spacers along the second silicon island.

46. The method of claim 1 wherein the first and second silicon forming steps are separate silicon forming steps.